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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,870	01/20/2004	Tai-Ho Wang	12049-US-PA	1869
31561	7590	10/03/2005	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN				BAUER, SCOTT ALLEN
		ART UNIT		PAPER NUMBER
		2836		
DATE MAILED: 10/03/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/707,870	WANG, TAI-HO
	<b>Examiner</b>	<b>Art Unit</b>
	Scott Bauer	2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-11 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_ is/are allowed.  
 6) Claim(s) 1-11 is/are rejected.  
 7) Claim(s) \_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 20 January 2004 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |                                                                                                                        |                                                                             |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. ____                                                 |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|                                                                                                                        | 6) <input type="checkbox"/> Other: ____.                                    |

## DETAILED ACTION

### ***Claim Objections***

1. Claim 4 is objected to because of the following informalities: Claim 4 contains the phrase, "wherein the ESD protection circuit is coupled to a second of the integrated circuit". The phrase should be changed to read: "wherein the ESD protection circuit is coupled to a second **pad** of the integrated circuit". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (US 6351364).

4. With regard to Claim 11, Chen et al., in Figure 2, discloses an electrostatic discharge (ESD) protection circuit (30) coupled to a pad of an integrated circuit (32), the integrated circuit having a system voltage (VDD) and a ground voltage (VSS) , the ESD protection circuit comprising: a P-type transistor (44), a first S/D terminal and a gate terminal of the P-type transistor coupled to the system voltage, a second S/D terminal of

the P-type transistor coupled to the pad; a first N-type transistor (40), a first S/D terminal of the first N-type transistor coupled to the system voltage, a gate terminal of the first N-type transistor coupled to the ground voltage, a second S/D terminal of the first N-type transistor coupled to the pad; and a second N-type transistor (38), a first S/D terminal of the second N-type transistor coupled to the pad, a gate terminal and a second S/D terminal of the second N-type transistor coupled to the ground voltage.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1 & 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6351364) in view of Okitaka (4858055).

7. With regard to Claims 1&2, Chen et al. in figure 2, teaches an ESD protection circuit, wherein an S/D terminal of a PFET (44) is connected to a pad (32), and the other S/D terminal and gate are connected to a first voltage. Chen et al. also teaches an S/D terminal of an NFET (40) connected to the pad, the second S/D terminal connected to a second voltage and the gate connected to ground. Chen et al. further teaches a second

NFET (38) wherein an S/D terminal is coupled to the pad via forth NFET transistor, and the gate and second S/D terminal are connected to ground.

Chen et al. does not teach connecting a diode in series with the PFET.

Okitaka, in Figure 2, teaches a diode (3) in series with a PFET (12) and power, wherein the cathode is coupled to power, and the anode is coupled to the PFET.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen et al. with Okitaka by placing a diode in series with the first PFET for the purpose of preventing current flow through the PFET (44) to the internal circuitry when a surge voltage is not present.

8. Claims 3, 7 & 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6351364) in view of Okitaka (4858055) and further in view of Miller et al. (US 6327126).

9. With regard to Claim 3 Chen et al. in view of Okitaka teach the ESD protection circuit as describe above.

Chen et al. in view of Okitaka do not teach an ESD protection circuit wherein two diodes are connected between a common voltage and ground. Miller et al., in Figure 6, teaches an electrostatic discharge circuit wherein the cathode of a diode (624) and the anode of another diode (626), are coupled to a common voltage (607), and the anode of the diode (624) and the cathode of the diode (626) are connected to a ground voltage (606).

In this configuration, the circuit is provided with a second diode (624) and a third diode (626), which are connected as required by the claim.

It would have been obvious to one of ordinary skill in the art at the time the invention was made, to combine the teachings of Chen et al. in view of Okitaka with Miller for the purpose of providing ESD protection to the negative power rail.

10. With regard to Claims 7 & 8, Chen et al. teaches an ESD protection circuit, wherein an S/D terminal of a PFET (44) is connected to a pad (32), and the other S/D terminal and gate are connected to a first voltage. Chen et al. also teaches an S/D terminal of an NFET (40) connected to the pad, the second S/D terminal connected to a second voltage and the gate connected to ground. Chen et al. further teaches a second NFET (38) wherein an S/D terminal is coupled to the pad via a third NFET transistor, and the gate and second S/D terminal are connected to ground.

Chen et al. does not teach connecting a diode in series with the PFET.

Okitaka, in Figure 2, teaches a diode (3) in series with a PFET (12) and power, wherein the cathode is coupled to power, and the anode is coupled to the PFET.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen et al. with Okitaka by placing a diode in series with the first PFET for the purpose of preventing current flow through the PFET (44) to the internal circuitry when a surge voltage is not present.

Chen et al. Further does not teach an ESD device wherein a diode is connected in series with an NFET. Miller et al., in Figure 6, teaches a diode where the cathode is

connected to a first common voltage and the anode is connected to a second common voltage.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen et al. with Miller by placing a diode in series with the second NFET for the purpose of preventing current flow through the NFET (38) to the internal circuitry when a negative surge voltage is not present.

11. Claims 4-6, 9 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Okitaka and Miller et al. (US 6327126) and further in view of Miller et al. (US 6724603).

12. With regard to Claims 4-6, Chen et al. in view of Okitaka and Miller et al. (US 6327126) teach the ESD protection circuit as described above in Claims 1-3.

Chen et al. in view of Okitaka and Miller et al. do not teach repeating the circuit of Claims 1-3 for a different I/O pad, as described in Claims 4-6 wherein both circuits share common bus lines. However, Miller et al. (US 6724603), in Figure 2, teaches an ESD protection circuit similar to the circuit taught in Claims 1-3. Miller et al., in Figure 2, further teaches that the ESD protection circuit has a plurality of I/O pads, and that each pad is protected by an identical ESD circuit wherein all protection circuitry share a common bus line.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen et al. Okitaka and Miller et al.

(US 6327126) with Miller et al. (US 6724603) for the purpose of providing ESD protection for every I/O pad contained on a chip.

13. With regard to Claims 9 & 10, Chen et al. in view of Okitaka and Miller et al. (US 6327126) teach the ESD protection circuit as described above in Claims 7 & 8.

Chen et al. in view of Okitaka and Miller et al. do not teach repeating the circuit of Claims 7 & 8 for a different I/O pad, as described in Claims 9 & 10 wherein both circuits share common bus lines. However, Miller et al. (US 6724603), in Figure 2, teaches an ESD protection circuit similar to the circuit taught in Claims 7 & 8. Miller et al., in Figure 2, further teaches that the ESD protection circuit has a plurality of I/O pads, and that an identical ESD circuit, wherein all protection circuitry share a common bus line, protects each pad.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen et al. Okitaka and Miller et al. (US 6327126) with Miller et al. (US 6724603) for the purpose of providing ESD protection for every I/O pad contained on a chip.

### ***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ker et al. (US 5631793) teaches an ESD protection circuit, wherein a pad is protected by a PMOS device where its gate and source are connected

to VDD and its drain is connected to the pad. Ker et al. also teaches an NFET wherein its gate and source are connected to ground, and its drain is connected to the pad.

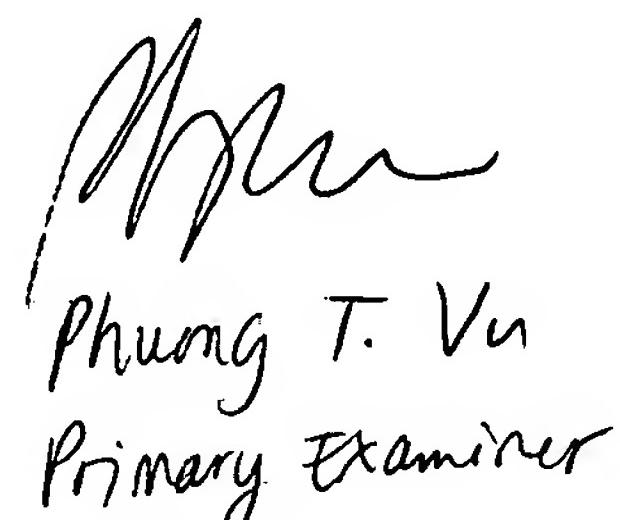
15. It is also noted that in Figure 2, the applicant discloses prior art, wherein an ESD protection circuit is provided for each pad, and that all protection circuitry share a common bus line.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB



Phuong T. Vu  
Primary Examiner